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# A SINGLE STAGE MOSFET BASED TRANSFORMERLESS INVERTER FOR NONISOLATED GRID TIED PV INVERTER APPLICATIONS

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**ABSTRACT**

This paper presents a single-phase leg splitted transformerless inverter. The transformerless PV inverter does not have a galvanic insulation. The parasitic capacitance between the PV array and ground results the high-frequency common mode voltage. This increases the power loss and reducing the grid current quality. The addition of two ac side switches in the inverter decouples the PV array from the grid, thus reducing the common mode voltage. The proposed inverter utilizes two filter inductors in both positive and negative half grid cycles. Thus, the inverter almost achieves full utilization of magnetics, and it reduces the cost and volume. The split structure of the proposed inverter thus not leads itself to reverse recovery issues for the main power switches. The PWM technique is used for the switching, and the results are simulated using MATLAB.

**Index Terms—** *Transformerless inverter, common mode voltage, MOSFET body diode reverse recovery, phase leg splitting inductor, PWM techniques.*

## I. INTRODUCTION

Nowadays, a most power that is used to meet our daily needs is obtained from fossil fuels. Owing to increases in consumption, fossil fuel sources may be exhausted shortly. But the use of fossil fuel has led to greenhouse gas emissions and environmental pollution. PV power generation systems have been regarded as the most promising future sources of energy because of their advantages, such as the absence of a need for fuel and the associated cost saving, low maintenance, and lack of noise. In PV microinverters galvanic isolation is not mandatory [1] – [4]. Fig. 1, shows a nonisolated architecture with high boost ratio dc-dc converter, which boosts PV panel and transformerless inverter gives 230 V grid voltages.[5] - [9]

To minimize common-mode voltage, the transformerless inverter at the secondary stage of the nonisolated PV microinverter is concentrated in this paper

## II. PROPOSED TRANSFORMERLESS INVERTER WITH ITS OPERATING MODES

### *A. Proposed Transformerless Phase leg Splitted Inverter*

This paper proposes a MOSFET based phase leg splitted inverter to reduce the MOSFET failure risk from body diode reverse recovery [10]. Fig. 2(a) shows a proposed inverter with separated magnetics and Fig. 2(b) shows a proposed inverter with an integrated magnetics.

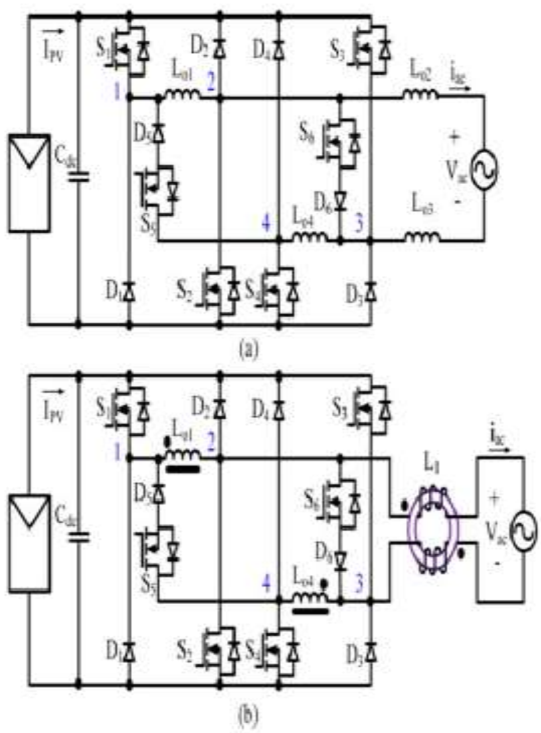


**Fig. 2. Proposed transformerless inverter topology with (a) separated magnetics and (b) integrated magnetics.**

One proposed phase leg is makeup by S , $S_2$ , $D_1$, $D_2$, and $L_{01}$ and another proposed phase leg is make up by $S_3$ , $S_4$ , $D_3$ , $D_4$, $L_{02}$. A freewheeling loop for positive current is provided by $S_5$, $D_5$ and a freewheeling loop for negative current is provided by $S_6$, $D_6$. $L_{01}$ and $L_{04}$ are phase leg splitting inductor designed for suppression of di/dt, and $L_{02}$ and $L_{03}$ are filter inductor. $L_{02}$ and $L_{03}$ are conducted both positive and negative half cycle. So it have 100% magnetic utilization but $L_{01}$ and $L_{04}$ are conduct only in the positive half cycle, so it has 50% utilization. Thus, the value of $L_{01}$ and $L_{04}$ are much smaller than the value of $L_{02}$ and $L_{03}$. PWM dead time does not need in the proposed inverter, only has two devices in the conduction loss, and has no risk from the reverse recovery of MOSFET body diode.

### *B. PWM Switching Method for Proposed Inverter*

Fig. 3 shows the circuit of PWM implementation for the proposed transformerless inverter.

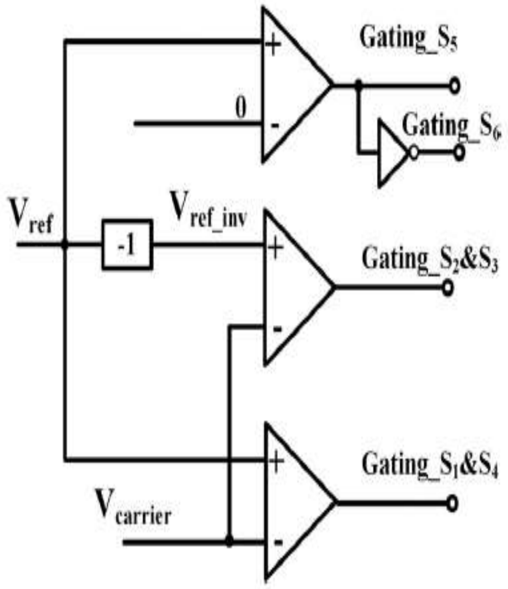


**Fig.3. PWM implemented circuit for the proposed inverter.**

$S_1$ and $S_4$ are simultaneously switched at in high frequency, which are driven by the output signal from the Comparison of the reference voltage $V_{ref}$ with carrier voltage $V_{carrier}$. In the entire positive half cycle, $S_5$ is turned on, which is driven by the output signal from the Comparison of $V_{ref}$ with 0. $S_2$ and $S_3$ are simultaneously switched at in high frequency, which are driven by the output signal from the comparison of $V_{inv\_ref}$ with $V_{carrier.}$ In the entire negative half cycle, $S_6$ is turned on, which is driven by the compliment output signal from the comparison of $V_{ref}$ with 0.

Dead time does not need for all PWM, so the implemented PWM has 100% duty cycle utilization [11]. This is because, one MOSFET in high switching frequency in a phase, another one MOSFET is in off state [12] – [15].

### *C. Modes of Operation for Proposed Inverter*

The proposed inverter has four operating modes in one grid cycle, and it was shown in Fig. 4.

**Mode 1:** As shown in Fig. 4(a), $S_1$ and $S_4$ are switched on; $D_5$ is reverse-biased, so the output current flows through $S_1$ and $S_4$ even though $S_5$ is turned on.

**Mode 2:** As shown in Fig. 4(b), $S_1$ and $S_4$ are switched off; $D_5$ is forward-biased, thus, the freewheeling current flows through $S_5$ and $D_{5.}$ Thus, PV is isolated from the grid in this mode of operation [16] – [20].

**Mode 3:** As shown in Fig. 4(c), $S_2$ and $S_3$ are switched on; $D_6$ is reverse-biased, so the output current flows through $S_2$ and $S_3$ even though $S_6$ is turned on

**Mode 4:** As shown in Fig. 4(d), $S_2$ and $S_3$ are switched off; $D_6$ is forward biased, thus, the freewheeling current flows through $S_6$ and $D_{6.}$ Thus PV is isolated from the grid in this mode of operation.

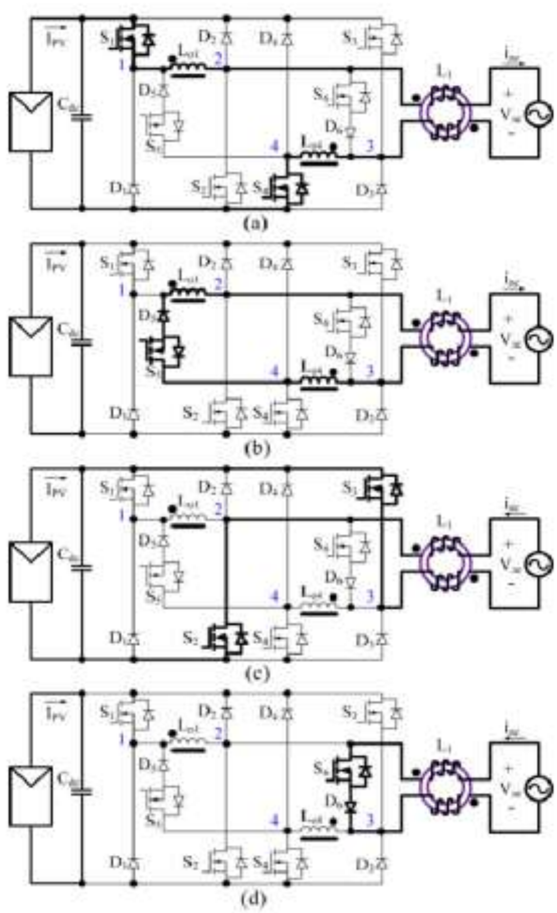

**Fig. 4. Operating modes of the proposed transformerless inverter: (a) positive half cycle, $S_1$ and $S_4$ are on, (b) positive half cycle, $S_1$ and $S_4$ are off, freewheeling current goes through $S_5$ and $D_5$ , (c) negative half cycle, $S_2$ and $S_3$ are on, and (d) negative half cycle, $S_2$ and $S_3$ are off, freewheeling current goes through $S_6$ and $D_6$.**

## III. SIMULATION RESULTS

The feasibility of the proposed MOSFET transformerless inverter for nonisolated microinverter applications was verified with MATLAB. A commercially available software package for power electronic simulations and proposed inverter was simulated based on following specifications:

**TABLE I**
**PARAMETERS OF THE PROPOSED TRANSFORMERLESS INVERTER**

| Components | Symbol | Value |
|---|---|---|
| Phase leg splitting inductor | $L_{01}$, $L_{04}$ | 0.086 mh |
| Output filter inductor | $L_{02}$, $L_{03}$ | 4.7 mh |
| Load resistance | $R_{load}$ | 220 ohm |
| Input voltage | $V_{in}$ | 340 V |
| Input current | $I_{in}$ | 12.5 A |
| Output voltage | $V_0$ | 220 V |
| Output current | $I_0$ | 1.04A |
| Output power | $P_0$ | 250 W |

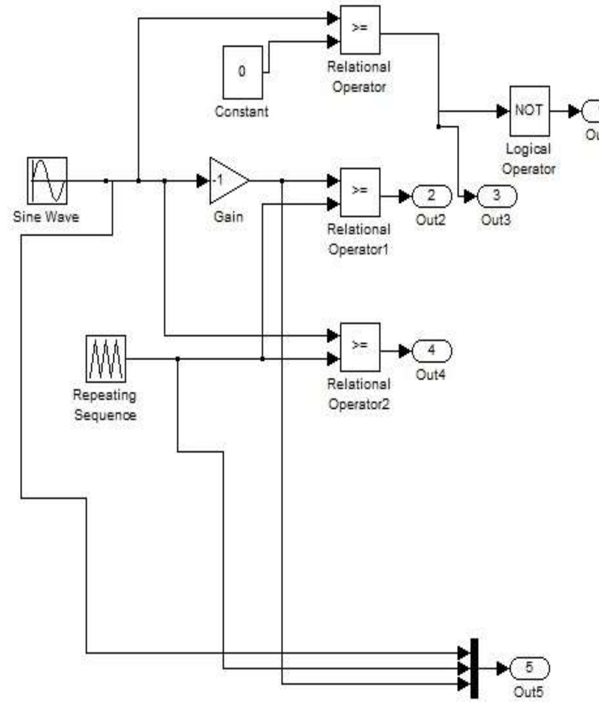


**Fig. 5. Simulation diagram of implemented PWM**

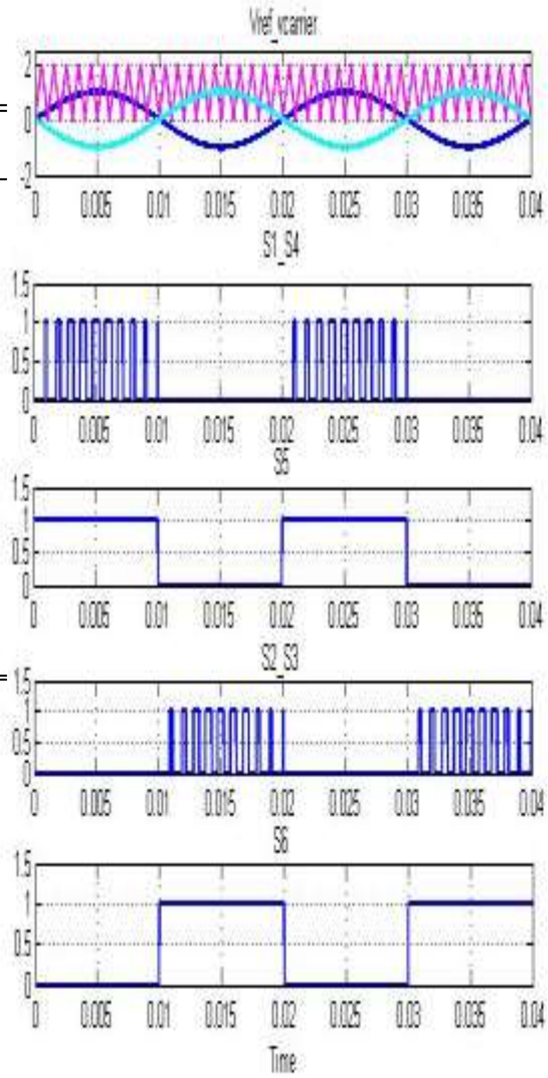


**Fig. 6. Simulated PWM signals for the proposed inverter**

Fig.5 shows the MATLAB simulation circuit of the PWM implemented circuit scheme for the proposed transformerless inverter. Fig.6 shows the gating signals for all switches. In the positive half cycle, $S_1$ and $S_4$ are simultaneously in high- frequency PWM and $S_6$ is continuously ON. Other switches are in OFF state. In the negative half cycle, $S_2$ and $S_3$ are switched simultaneously in high-frequency PWM and $S_6$ is continuously ON. Other switches are in OFF state.

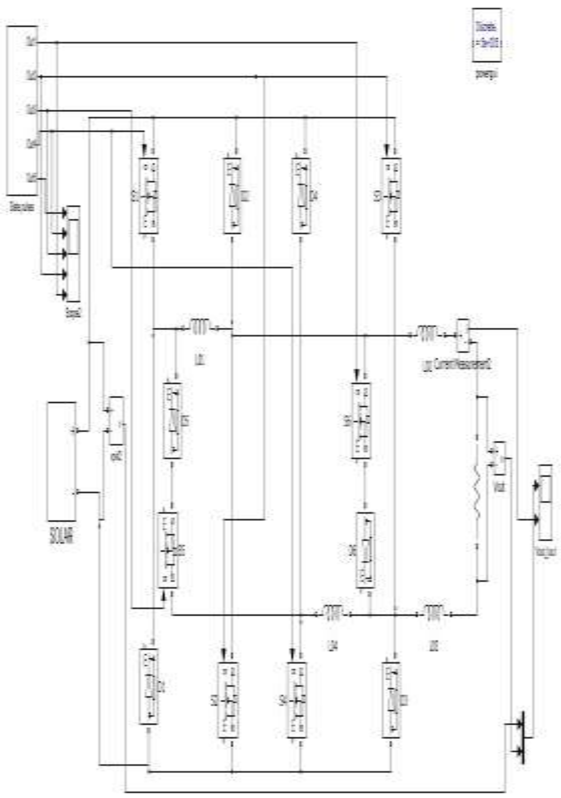


**Fig. 7.Simulation diagram for proposed MOSFET based inverter**

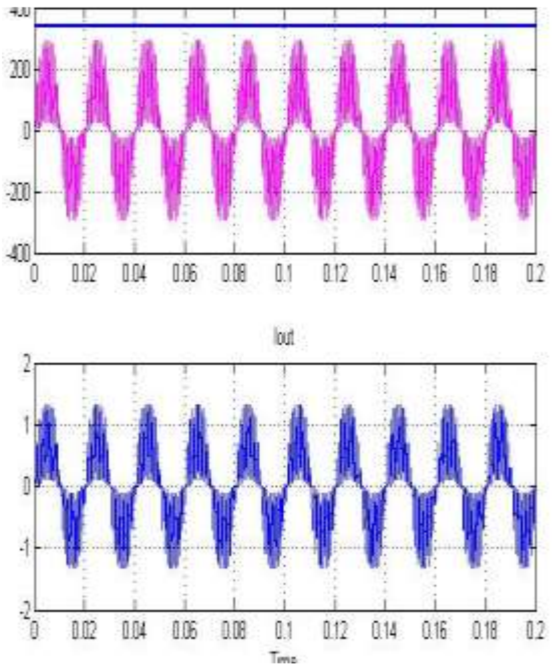


**Fig. 8. Simulated waveform of proposed output voltage and output current**

MATLAB simulation diagram for the proposed inverter is shown in Fig. 7. This contains two filter inductors about 4.7 mH and phase leg splitted inductors about 0.086 mH. The proposed inverter has two ac side switches conduct through the diode. The output voltage and current waveforms of the proposed inverter are shown in Fig.8. As there is no dead time requirement for each PWM switching cycle, the proposed inverter has no duty cycle loss, which means 340 V dc bus can almost generate 220 V ac voltage.

## IV. CONCLUSION

This paper proposed a phase leg splitted non-isolated transformerless inverter, which achieves high magnetic utilization and low common mode voltage. The proposed transformerless inverter has no dead time requirement for each PWM switching cycle; the inverter has no duty cycle loss. It generates 220 V, 50 HZ ac from the 340 V solar input. The inverter output current is 1.5 A. Due to the advantages of low common mode voltage and improved magnetic utilization, the proposed topology is attractive for non-isolated PV microgrid applications and transformerless string inverter applications.

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